The NBTI Impact on RF Front End in Wireless Sensor Networks

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***Abstract*—The life time of RF front end in Wireless Sensor Networks (WSN) is so important that it decides whether the whole system can work normally for a long time. Under CMOS technology, Negative Bias Temperature Instability (NBTI) is one of the most important factors that decide chips' life time. Especially with the feature size declining, NBTI effect is becoming more and more serious. Previous works mainly focus on NBTI effect at device level, or NBTI effect in large-scale digital circuits. In this paper, for the WSN node, we study the NBTI impact on the front-end circuits, such as Voltage-Controlled Oscillators (VCO), Charge Pump (CP), Low Noise Amplifier (LNA), and the whole transceiver system. The circuit level NBTI degeneration models are built for the key modules and the entire transceiver. The mathematical models can be summarized into a conclusion that the phase noise of the VCO will deteriorate, the current mismatch of the CP and the noise figure of the LNA will both increase, and then the sensitivity and Adjacent Channel Selectivity (ACS) will be depressed by NBTI. Under HJTC 0.18-μm technology, our conclusions are proved by the simulation results.**

I. Introduction

As early as the MOSFET appears, people found the Negative Bias Temperature Instability (NBTI) mechanism. Goetzberger's team was the first to give a detailed description of negative bias and temperature pressure [1]. With the process feature size decreasing, the thickness of gate oxide is declining. The effect of NBTI is inversely proportional to gate-oxide thickness, so the performance degrade of device will be more serious. NBTI has an impact on both PMOSFETs and NMOSFETs. However, PMOSFETs suffer more, so people mainly focus on the NBTI effect of PMOSFETs, especially the NBTI impact on PMOS large-scale digital circuits. In recent years there are also some papers about the NBTI effect in analog and RF circuits [2]–[5]. Some of them give the simulation results of simple circuits such as current mirrors and OperaTional Amplifiers (OTA), in which mismatch is caused by NBTI effect [2], [3]. Neeraj analyzed the reliability of analog circuits such as OTAs and digital-to-analog converters under NBTI [4]. Christian gave a simple forecast on the performance degeneration of OTAs and Voltage-Controlled Oscillators (VCO) [5] caused by NBTI. However, none of them have made a detailed mathematical analysis at the circuit level; the lack of qualitative analysis and circuit level mathematical models is still a problem. Furthermore, there is no paper showing a comprehensive research of NBTI impact on a whole transceiver system.

For the RF front end in Wireless Sensor Networks (WSN) systems, power consumption, life time, and dynamic range are the three most critical specifications. And the life time of RF front end is very important for WSN since the nodes may need to send and receive data for many years in some applications. Under CMOS technology, the chips' life time is mainly decided by NBTI, especially with the feature size declining. And NBTI brings aging or even failure to the RF front end in the communication nodes. So it's necessary to study the NBTI impact on the RF front end in WSN system.

In this paper, we choose the WSN transceiver as the target system, and focus on the NBTI impact on the performance of the key modules and the entire transceiver system. The contributions of this paper can be summarized into the following aspects:

- Provide a NBTI induced degeneration analysis methodology from mathematical models to simulation for RF front end.
- Build circuit level NBTI degeneration models for VCO, Charge Pump (CP), and Low Noise Amplifier (LNA); and study the impact on the whole WSN transceiver.
- Get the conclusion that the phase noise of the VCO will deteriorate, the current mismatch of the CP and the noise figure of the LNA will increase, and the sensitivity and Adjacent Channel Selectivity (ACS) will be depressed by NBTI.
- Give the NBTI induced performance declining quantity of the VCO, CP and LNA by simulation under 0.18-um technology, and estimate the performance degeneration of the entire transceiver by our mathematical models.

The rest of our paper is organized as follows. Section 2 gives an overview of our WSN transceiver design and the NBTI effect in the WSN transceiver. The NBTI models of VCO, CP and LNA are obtained in Section 3, Section 4 and Section 5 respectively. We simulate the NBTI impact on the key modules in Section 6. Section 7 concludes the paper.

II. An overview of the WSN transceiver

Taking high integration level and low power consumption into account, we choose the low-IF structure for our WSN transceiver. As shown in Fig.1, CF represents Complex Filter; IF contains demodulator, slicer, clock recovery and so on; BB represents Base-Band circuits; Mod represents Modulator. The RF frequency band for communication is from 430 MHz to 435 MHz, and the IF frequency is 200 KHz. In order to save chip area, the frequency band of the PLL is 1.72 GHz-1.74 GHz (quadruple frequency) for the realization of small inductor in VCO. As a result, the signals sent to PA and mixers are produced by a four module frequency divider after the Phase-Locked Loop (PLL). Our PLL is a conventional charge pump

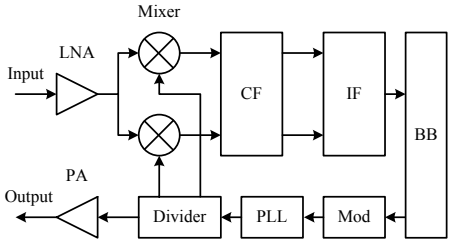

Fig. 1. The structure of the WSN transceiver.

PLL, which includes Phase Frequency Detector (PFD), CP, VCO, and Sigma-Delta Modulator (SDM).

Generally speaking, the NBTI effect in every module may have impact on the performance of the transceiver system. However,

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the NBTI effect in the three key modules (VCO, CP and LNA) depressed the transceiver's performance most. For WSN transceiver, a high sensitivity (< -100 dBm) is required for ultra far-distance transmission; the ISM band (430 MHz-435 MHz) is very narrow, but the channels required are too many, so a high ACS is required. VCO decides the noise performance and the power consumption of the PLL, the current mismatch of CP seriously increases the phase noise of the PLL, and ACS is decided by the phase noise of PLL. As a result, both the phase noise of VCO and the current mismatch of CP decide the ACS [6]. For LNA, the heart of receiver, the noise directly affects the sensitivity of the receiver [6].

In other parts such as mixers, complex filters, IF circuits and so on, the core circuit is OTA. All the OTAs are biased by a common current mirror, whose currents do not change under NBTI, so the transconductance of the input MOSFETs remains almost unchanged. And we leave a certain margin when designing the OTAs so that the input MOSFETs will not be cut off by NBTI effect. Then the NBTI impact on mixers, complex filters, and IF circuits can be neglected. Therefore, we only study the NBTI effect in the three key modules VCO, CP, and LNA.

III. The NBTI effect in VCO

In this part we give the circuit level NBTI induced phase-noise model of VCO based on Leeson's theories; and then we analyze the VCO's NBTI impact on PLL; at last the receiver's performance degeneration caused by VCO's NBTI induced degeneration is obtained in the form of mathematical models.

A. The NBTI induced phase-noise models of VCO

Based on Leeson's theories, the circuit level NBTI models are built here. For PMOSFET in strong inversion region, the threshold voltage variation caused by NBTI is [7]:

$$\Delta V_{th} = K_v^{2n} t^n + \delta_v \tag{1}$$

in which t is the length of time, δ_v is the initial change of the threshold voltage, and K_v is described in detail in paper [7]. As shown in Fig.2, the gate-to-source voltage of M1 and M2 is

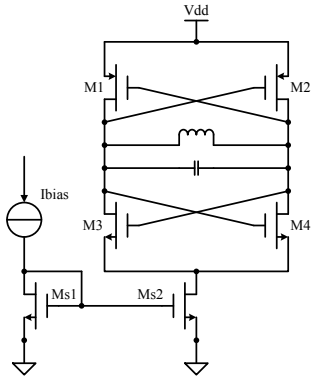

Fig. 2. The current-biased VCO.

$V_{gs} = V_{dd} - Vcm$, in which V_{cm} is the middle value of the VCO's output voltage. Although the output wave is a large signal, V_{cm} is approximately equal to the output DC voltage.

For the phase-noise model of VCO, according to Leeson's theory [8], the phase noise in the area of $1/f^2$ is [9]:

$$S_\phi(\omega_m) = \left(\frac{\omega_o}{2Q}\right)^2 \frac{2FkT}{P_s} \omega_m^{-2} \tag{2}$$

in which $\omega_o(rad/s)$ is the resonant frequency, q is the quality factor of LC tank, F is the effective noise figure, k is the Boltzmann constant, T is the absolute temperature, ω_m is the offset frequency. P_s is the power of the output signal, which is proportional to the output amplitude:

$$P_s = k_1 V_o^2 = k_1 (\frac{4IR}{\pi})^2 \tag{3}$$

in which k_1 is a constant, R is the equivalent parallel resistance of the LC tank. I is the average current injected to LC tank by the cross-coupled MOSFETs, which can be considered equal to the DC current I_{dc}. Then we can get the phase-noise model under NBTI effect:

$$S_\phi(\omega_m) = \frac{FkT(\pi\omega_o)^2}{32k_1(QR\omega_m)^2} \frac{1}{I_{dc}^2} \tag{4}$$

The threshold voltage of PMOSFETs M1 and M2 will be decreased by NBTI, and then the DC current I_{dc} will be reduced. As a result, the noise performance will be deteriorated according to equation (4).

B. VCO's NBTI impact on PLL

As NBTI effect causes the phase noise of VCO to increase, the phase noise of PLL will also be increased. The relationship between the phase noise of VCO and PLL is [10]:

$$\phi_{pll}(s) = \frac{s^2}{s^2 + 2\xi\omega_n s + \omega_n^2} S_\phi(\omega_m) \tag{5}$$

in which $s = j\omega_o$ (ω_o is the output frequency of VCO), and:

$$\omega_n = \sqrt{\frac{K_{vco} I}{2\pi C_p}}, \quad \xi = \frac{R}{2}\sqrt{\frac{K_{vco} I C_p}{2\pi}}$$

in which C_p is the capacitance of the loop filter in PLL [10] is the gain of VCO, R is the resistance of the loop filter [10], I is the pumping current of the charge pump.

We can see that transfer function (5) shows a high-pass character. Equation (4) shows the phase noise in the area of $1/f^2$ [9], so a great part of the increment in phase noise will be delivered to the output of the PLL.

Based on Leeson's theory, we can obtain the phase noise model of PLL according to (4) and (5):

$$\phi_{pll}(\omega_m) = \frac{\pi^2 FkT}{32k_1 Q^2 R^2 \omega_m^2} \frac{\omega_o^4}{\omega_o^2 - 2j\xi\omega_n\omega_o - \omega_n^2} \frac{1}{I_{dc}^2} \tag{6}$$

Equation (6) shows that an NBTI induced decrement in VCO's DC current will bring a phase-noise increment to PLL.

C. VCO's NBTI impact on receiver

The local oscillator signal is produced by PLL, so the ACS of the WSN transceiver is [6]:

$$\Delta S_{adj} = 10lg(\frac{10^{\frac{S_{d,i}-CNR}{10}} - 10^{\frac{-174+10lgBW+NF}{10}}}{10^{\frac{\phi_{pll}+10lgBW}{10}} + 10^{\frac{S_{pll}}{10}}}) - S_{d,i} \tag{7}$$

in which $S_{d,i}$ is the input test signal [6], CNR is the signal-to-noise ratio, BW is the bandwidth of the receiver, NF is the noise figure of the receiver, ϕ_{pll} is the phase noise of the PLL, S_{pll} is the spur of the PLL.

Then the ACS under VCO's NBTI effect can be obtained based on Leeson's models:

$$\begin{aligned} \Delta S_{adj} &= 10lg(\frac{A}{10^{\frac{BI_{dc}^{-2}+10lgBW}{10}} + 10^{\frac{S_{pll}}{10}}}) - S_{d,i} \\ A &= 10^{\frac{S_{d,i}-CNR}{10}} - 10^{\frac{-174+10lgBW+NF}{10}} \\ B &= \frac{\pi^2 FkT\omega_m^2}{32k_1 Q^2 R^2} \frac{\omega_o^4}{\omega_o^2 - 2j\xi\omega_n\omega_o - \omega_n^2} \end{aligned} \tag{8}$$

In summary, under NBTI effect, the DC current of VCO I_{dc} will be reduced, so the ACS of the receiver will be depressed.

IV. The NBTI effect in CP

As shown in Fig.3 [11], NBTI causes the threshold voltage of M1, M2, M5, and M6 to increase; as a result, the current mismatch of CP changes. As the gate-to-source voltages of M2 and M6 are much smaller than that of M5. And M1 is a switch, which works under recovery much longer than that under stress. So we neglect the NBTI effect on M1, M2, and M6.

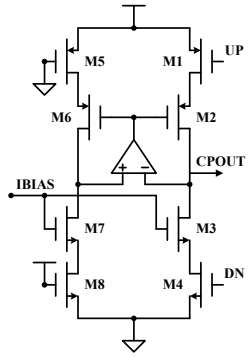

Fig. 3. The schematic of CP [11].

According to Mao's model [12], the phase noise of PLL can be described with the current mismatch:

$$\phi_{pll}(\omega_o) = \Big|\frac{T(\omega_o)}{1+T(\omega_o)}\rho_e\Big|^2 \big(\sigma(|\phi_{n,sdm}|)\big)^2 \frac{1}{f_{ref}} \tag{9}$$

in which ρ_e is the ratio of current mismatch, ω_o is the output frequency of the PLL, $T(\omega_o)$ is the open-loop gain, $\sigma(|\phi_{n,sdm}|)$ is the standard deviation of the data stream input into the sigma-delta modulator, f_{ref} is the reference frequency. As ρ_e will be increased by NBTI, a phase noise increment in PLL appears. Then the ACS under the impact of CP's NBTI is:

$$\Delta S_{adj} = 10lg\Big(\frac{A}{10^{\frac{C\rho_e^2+10lgBW}{10}} + 10^{\frac{S_{pll}}{10}}}\Big) - S_{d,i} \tag{10}$$
$$C = \Big|\frac{T(\omega_o)}{1+T(\omega_o)}\Big|^2 \big(\sigma(\phi_{n,sdm})\big)^2 \frac{1}{f_{ref}}$$

Through the model shown in equation (10), we can estimate the deterioration of receiver's ACS caused by the NBTI induced current-mismatch increment in CP.

V. The NBTI effect in LNA

As shown in Fig.4, the PMOSFETs Mp1, Mp2, Mp3 and Mp4 are switches used to control the gain of the LNA, whose threshold voltages will be increased by NBTI effect, and then the DC current I_{dc} will be decreased.

The Noise Figure (NF) of such source degenerated LNA is [13]:

$$F_{lna} = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s (\omega_o/\omega_T)^2 \tag{11}$$
$$NF_{lna} = 10lgF_{lna} \tag{12}$$

in which ω_o is the operating frequency, R_l is the resistance of the inductor at the input, R_s is the resistance of the signal source, R_g is the gate resistance of the input MOSFET, γ is a constant, g_{d0} is the transductance at zero bias, ω_T is the cut-off frequency of the input MOSFET:

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{\sqrt{2\mu_n C_{ox}(W/L)}}{C_{gs}}\sqrt{I_{dc}} \tag{13}$$

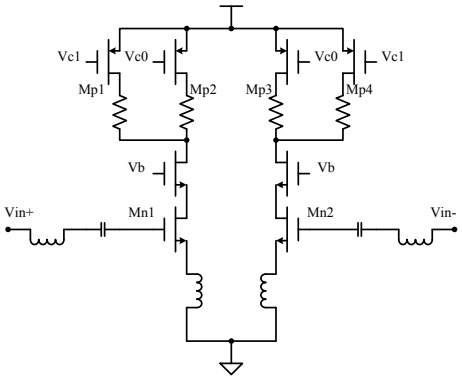

Fig. 4. The schematic of LNA.

in which g_m is the transductance of the input MOSFETs Mn1 and Mn2, C_{gs} is the gate capacitance of Mn1 and Mn2, μ_n is the mobility of electrons, C_{ox} is the unit area of gate capacitance, (W/L) is the width-to-length ratio of Mn1 and Mn2, I_{dc} is the DC current of LNA. NBTI caused the DC current I_{dc} to be reduced, so the NF of the LNA will be increased.

The noise figure of the LNA plays a decisive role in the noise performance of the entire receiver system. The noise figure of the receiver is:

$$NF_r = NF_{lna} + \frac{NF_{others}}{G_{lna}} \tag{14}$$

NF_{others} is the overall noise figure of other modules, G_{lna} is the gain of the LNA.

Then the sensitivity of the receiver can be obtained:

$$S_{min} = 10lg\Big[1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma g_{d0} R_s \omega_o^2 C_{gs}^2}{4\mu_n C_{ox}(W/L) I_{dc}}\Big] + D \tag{15}$$
$$D = -174 + 10lg(BW) + \frac{NF_{others}}{G_{lna}} + CNR_{min}$$

in which BW is the bandwidth of the receiver, CNR_{min} is the minimum signal-to-noise ratio.

Therefore, through equation (15), we can see that NBTI will reduce the DC current in LNA, which will increase the noise figure of the LNA, and then depresses the sensitivity of the receiver.

VI. Circuits designs and simulation results

Under HJTC 0.18μm technology, we design the key modules VCO, CP and LNA for WSN usage. Then we simulate the three key modules without NBTI and under NBTI respectively.

A. The simulation results of VCO

First we design a VCO as shown in Fig.2, the parameters in equation (1) for simulation are chosen as follows in Table I:

TABLE I
THE PARAMETERS ADOPTED FOR CALCULATE NBTI EFFECT IN VCO.

$V_{dd}(V)$	1.8	$\delta_v(mV)$	5.0
$t_{ox}(nm)$	10	$K_1(C^{-0.5}nm^{-2.5})$	7.5
$V_{th}(mV)$	458.5	$E_a(eV)$	0.49
$T(k)$	353	n	0.16
$q(10^{-19}C)$	1.6	$\varepsilon_{ox}(10^{-13}F/cm)$	3.5
$V_{gs}(mV)$	740.3	$E_{01}(V/nm)$	0.08
$k(10^{-23}J/K)$	1.38	$T_0(10^{-8}s/nm^2)$	1
$Technology$	$HJTC0.18\mu m$	$t(years)$	10

The results show that the change of threshold voltage is 6.1 mV. The simulation results is shown in Fig.5, and then are summed up in Table II.

The phase noise is increased by 1.1 dB at most, which proves the conclusion we get in section 3.

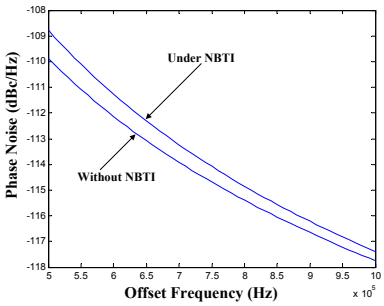

Fig. 5. The phase noise under NBTI and without NBTI.

TABLE II
THE SIMULATION RESULTS OF VCO.

$Phase\ Noise$	$500KHz\ offset$	$1MHz\ offset$
$Without\ NBTI$	$-109.881\ dBc/Hz$	$-117.7504\ dBc/Hz$
$Under\ NBTI$	$-108.7738\ dBc/Hz$	$-117.3907\ dBc/Hz$

B. The simulation results of CP

We design a CP according to Lee's architecture [11], as shown in Fig.(3), all the parameters for simulation are chosen the same as in Table I except for three ones: $t_{ox} = 4.2nm$, $V_{th} = 442.1mV$, $V_{gs} = 1.784V$.

The change of M5's threshold voltage is 15.9 mV. The simulation results are shown in Fig.(6). As the control voltage of VCO is from 0.4 V to 1.2 V, we only need to study the current mismatch on the condition of the output voltage changing from 0.4 V to 1.2 V. The maximum current mismatch is summed up in Table 4.

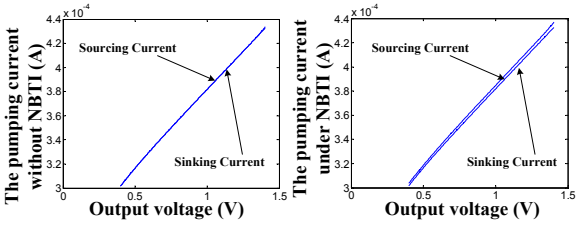

Fig. 6. The current mismatch of CP under NBTI and without NBTI.

TABLE III
THE MAXIMUM CURRENT MISMATCH OF CP.

$Maximum\ Current\ Mismatch\ Ratio$	$Without\ NBTI$	$Under\ NBTI$
	0.21348%	0.98384%

We can see that the current mismatch ratio is increased to about 4.6 times. According to the models built by Mao Xiaojian [12], the phase noise of the PLL will be increased by about 13 dB.

C. The simulation results of LNA

We design a LNA as shown in Fig.(4). In order to decrease the chip area, non-integrated inductor is adopted here since the operating frequency is not very high. We use murata's model [14] for simulation. All the parameters for simulation are chosen the same as in Table I except for three ones: $t_{ox} = 10nm$, $V_{th} = 513.9mV$, $V_{gs} = 1.8V$.

The calculation results show that the change of PMOSFETs' threshold voltage is 9.1 mV. The simulation curves of NF are shown in Fig.(7).

The maximum increment of NF under NBTI is about $3.04 \times 10^{-5} dB$, which means that our forecast on the degeneration of LNA's NF in section 5 is reasonable.

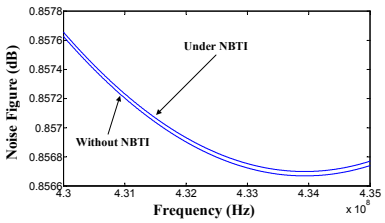

Fig. 7. The NF of the LNA under NBTI and without NBTI.

VII. CONCLUSION

NBTI decreases the life time of the front end in WSN nodes. We analyze the NBTI impact on VCO, CP, LNA and the whole WSN transceiver system in this paper. Both the mathematical analysis and the circuit simulation results show that under NBTI the phase noise of the VCO will be deteriorated, the current mismatch of CP and the noise figure of the LNA will be both increased. All these will worsen the ACS and the sensitivity of the receiver. And the NBTI effect in CP give the most serious impact, which even lead to a merely 13 dB increase of PLL's phase noise. As a result, the ACS of the WSN receiver will be depressed a lot. Please note that the technology we used is 180-nm, although the NBTI effect on LNA is not very obvious, the noise performance of LNA will deteriorate much more under the technology with smaller feature size, because the threshold voltage will be increased more by NBTI under advanced technology. So the performance degeneration of the 180-nm circuits and systems give a forecast on further research. For future work, we will design the transceiver system under the condition that some margin is left for NBTI effect; and we will try to design some compensation circuits to deal with NBTI.

REFERENCES

[1] A. Goetzberger and H. E. Nigh, "Surface charge after annealing of al-sio2-si structures under bias," *Proceedings of the IEEE Proceedings of the IEEE Proceedings of the IEEE*, vol. 54, no. 10, pp. 1454– 1454, 1966.

[2] P. Chaparala, D. Brisbin, and J. Shibley, "Nbti in dual gate oxide pmosfets," in *Plasma- and Process-Induced Damage, 2003 8th International Symposium*, ser. Plasma- and Process-Induced Damage, 2003 8th International Symposium, 2003, pp. 138– 141.

[3] M. Agostinelli, S. Lau, S. Pae, P. Marzolf, H. Muthali, and S. Jacobs, "Pmos nbti-induced circuit mismatch in advanced technologies," in *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, ser. Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International, 2004, pp. 171– 175.

[4] N. K. Jha, P. S. Reddy, D. K. Sharma, and V. R. Rao, "Nbti degradation and its impact for analog circuit reliability," *Electron Devices, IEEE Transactions on Electron Devices, IEEE Transactions on*, vol. 52, no. 12, pp. 2609– 2615, 2005.

[5] C. Schl, R. Brederlow, B. Ankele, W. Gustin, K. Goser, and R. Thewes, "Effects of inhomogeneous negative bias temperature stress on p-channel mosfets of analog and rf circuits," *Microelectronics Reliability*, vol. 45, no. 1, pp. 39–46, 2005.

[6] Q. Gu, *RF System Design of Transceivers for Wireless Communications*. Springer Science+Business Media, LLC, 2005.

[7] W. Wenping, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and C. Yu, "An integrated modeling paradigm of circuit reliability for 65nm cmos technology," in *Custom Integrated Circuits Conference, 2007. CICC '07. IEEE*, ser. Custom Integrated Circuits Conference, 2007. CICC '07. IEEE, 2007, pp. 511–514.

[8] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329– 330, 1966.

[9] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *Solid-State Circuits, IEEE Journal of*, vol. 33, no. 2, pp. 179–194, 1998.

[10] B. Razavi, *RF Microelectronics*. PEARSON EDUCATION ASIA LIMITED and TSINGHUA UNIVERSITY PRESS, 2003.

[11] J. S. Lee, M. S. Keel, S. I. Lim, and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," *ELECTRONICS LETTERS*, vol. 36, no. 23, pp. 1907–1908, 2000.

[12] M. Xiaojian, "Design and analysis of sigma-delta fractional-n phase-locked loop frequency synthesizer," Ph.D. dissertation, Tsinghua University, 2006.

[13] D. K. Shaeffer and T. H. Lee, "A 1.5-v, 1.5-ghz cmos low noise amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 5, pp. 745–759, 1997.

[14] murata, "http://www.murata.com/," 2008.